The next generation FrontEnd Controller for the Phase 1 Upgrade of the CMS Hadron Calorimeters

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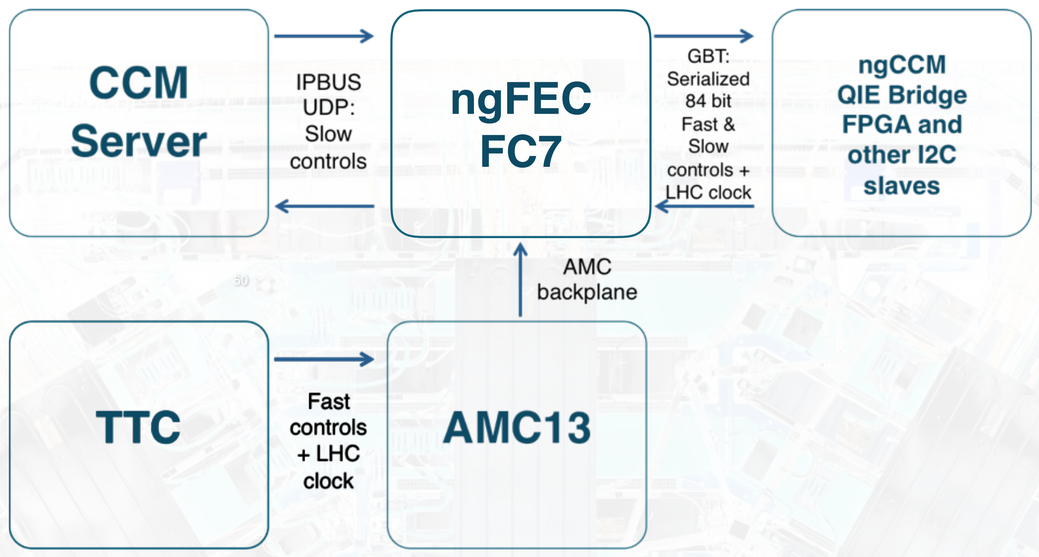
Abstract: The ngFEC (next generation FrontEnd Controller) is the system responsible for slow and fast control within the Phase 1 Upgrade of the CMS Hadron Calorimeters. It is based on the FC7, a µTCA compatible Advanced Mezzanine Card developed at CERN and built around the Xilinx Kintex®-7 FPGA. The ngFEC decodes the 40.0788 MHz LHC clock and the synchronization signals received from the backplane and distributes them to the frontend electronics using a GBT link. The latency of the fast control signals is fixed across power cycles and across identical ngFEC channels. Even if the direct link to a frontend module is broken, a redundancy scheme ensures a successful communication using the link to the neighboring frontend module. Thanks to the ngFEC all frontend modules can be remotely programmed through the JTAG standard. The CCM server software interfaces the ngFEC to the Detector Control System (DCS) which constantly monitors voltages and temperatures on the frontend electronics. This contribution reviews the characteristics and the development status of the ngFEC.

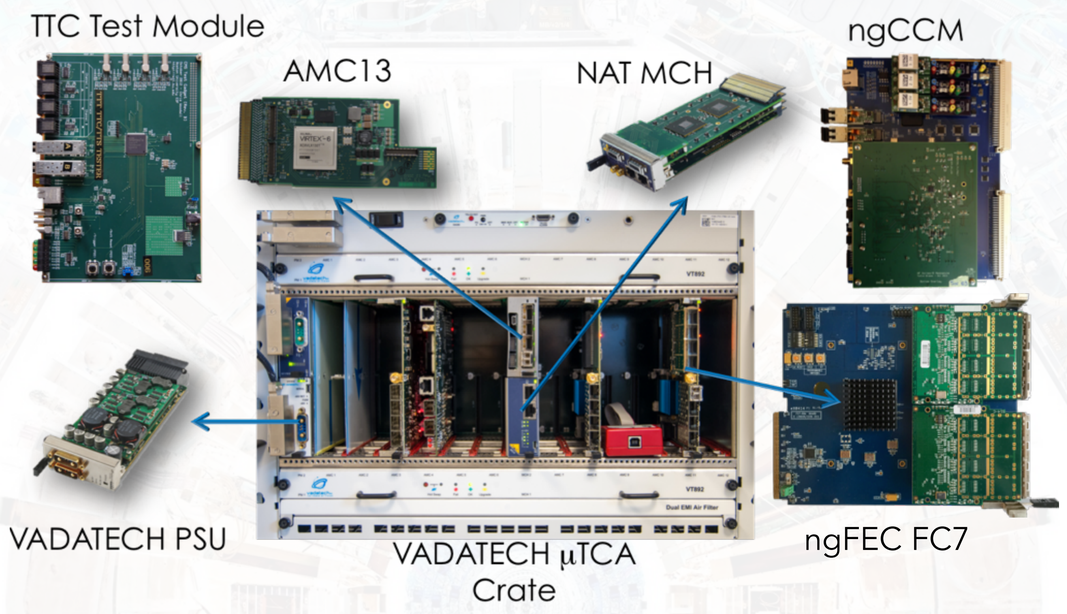
Introduction

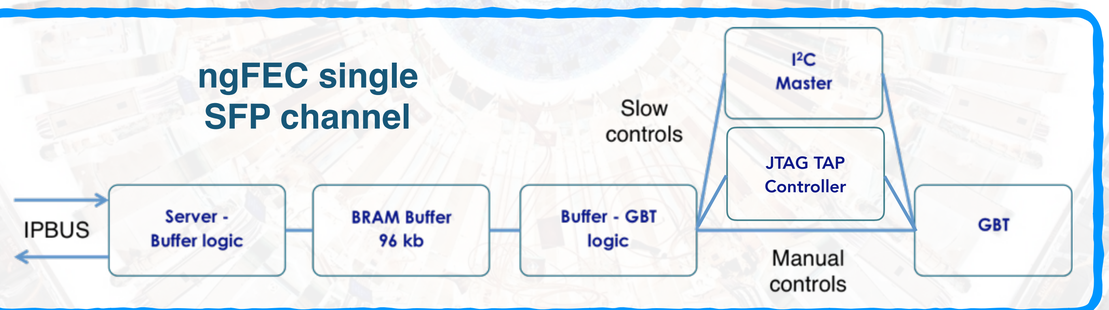
The energy and luminosity upgrade of the Large Hadron Collider (LHC) and Compact Muon Solenoid (CMS) Detector requires improvements on the CMS electronic infrastructure as well. The CMS HCAL control system is planned to be upgraded by

- replacing VME standard to μTCA which offers higher data transfer rates through the backplane, better cooling options, and power management configurations in a more compact crate;
- adding redundant control paths between the front end crates;
- improving software and firmware features, reliability, and performance.

The next generation Front-End Control (ngFEC) crate connects and organizes the control path between the front-end modules and the CMS control systems. It also distributes the LHC clock (40.0788 MHz) to the front-end readout system.







Advanced Mezzanine Card 13 (AMC13): Collects and distributes DAQ, TTC and TTS information to the modules within µTCA crate; developed by Boston University.

FMC carrier - Xilinx Series 7 (FC7): flexible, µTCA compatible AMC for generic data acquisition/control applications. Built around the Xilinx Kintex®-7 FPGA, the FC7 provides developers with a platform which has access to a large array of configurable I/O, primarily delivered from onboard FPGA Mezzanine Card (FMC) headers. Targeting users of high speed optical links in high energy physics experiments, the board can drive and receive links up to 10Gb/s.

Next Generation Clock Control Module (ngCCM): The clocks will be distributed to the front end modules by ngCCM. It is a replacement for the old CCM module and it is developed by UVA and CERN.

IPBUS Protocol: A reliable IP-based protocol for controlling ATCA/μTCA modules, which enables the use of UDP packets to establish the communication between the CCM Server and the ngFEC FC7.

GigaBit Transceiver (GBT) Protocol: A transmission protocol targeting high speed data transfer in radiation-harsh environments of high energy experiments.
It provides three different encoding schemes with different error correction and detection capabilities: “GBT-frame”, “8b10b” and “Wide-Bus”. Following the different encoding schemes, the GBT protocol serializes and deserializes 120 bit frames (88 bits or 84 bits effective including slow controls) and can achieve up to 4.8 Gbit/s transfer speed.
The “GBT-Frame” encoding scheme is implemented in the ngFEC FC7 firmware.

ngFEC FC7

Each ngFEC FC7 is capable of controlling 6 HF (HB/HE) front-end modules each with 14 (12) I²C slaves. Each μTCA crate can accomodate up to 12 ngFEC FC7s.

Slow control, JTAG, and ngFEC specific commands are received from the CCMServer through IPBUS protocol and stored in dual port BRAM blocks. The fast controls coming from TTC through the AMC13 are directly sent to ngCCM.

The ngFEC crate communicates with the ngCCM via GBT protocol through the fiber connections. Each I²C master on the ngFEC FC7 controls one bit of the GBT word and all the masters are sharing the same I²C clock. Therefore, even though the data transfer rate is 4.8 Gbit/s, 100 KHz I²C communication can be maintained simultaneously and independently for each front-end I²C slave.

CCM Server and TTC

Crate Control Module (CCM) Server is developed at DESY. The CCM server sets the configure/enables the front-end modules. It also reads the debugging and the sensor information (temperature, voltage, etc) from the front-end modules and drives the manual controls like reset signals.

The CCM Server forms slow control commands and sends them to ngFEC FC7 board through the IPBUS protocol.

Right now, the CCM Server provides a command line interface, and a GUI will be implemented in the future as well.

The central LHC clock and fast controls delivered by the **Timing Trigger Control (TTC)** system to the AMC13 board in the ngFEC crate. The AMC13, then, recovers the fast control signals and 40.0788 MHz LHC clock from the SFP connection and distributes them to the ngFEC FC7s.

Front-End Electronics

The front-end modules are located next to/inside the CMS detector, hence they must be able to operate in a harsh radiation environment.

The ngCCM distributes the fast control commands, the LHC clock and the slow control commands to the front-end. An internal I²C slave sends temperature and status information to the CCM server.

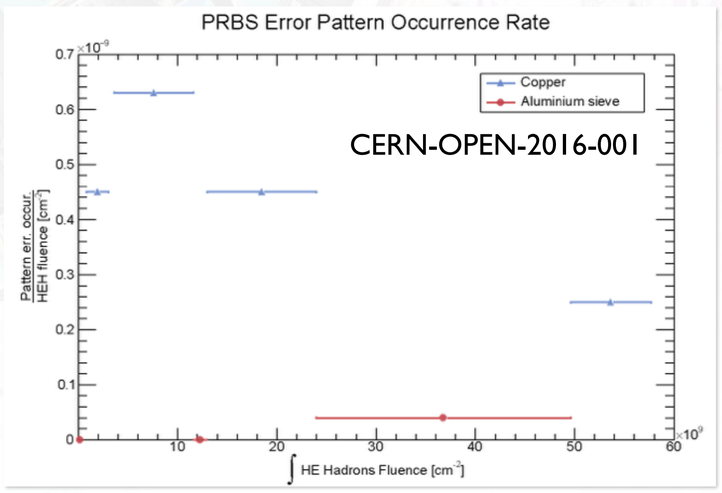
The QIE boards carry a bridge FPGA which provides access to several components on the board (QIE, GBTx chips etc). An I²C slave implemented on the bridge FPGA with a custom scheme between the CCM Server and the bridge FPGA routes the slow control commands to other components by switching I²C lines. Therefore, the CCM Server effectively controls all the components on each QIE board with a single I²C link to the board.

Irradiation test at CHARM, CERN

An error detection module is designed in the FPGAs on the two sides of the link using 23-bit Pseudo Random Binary Sequence (PRBS). The generated 23-bit PRBS patterns are included in the payload of the link in both directions. This module is employed to detect the errors that could not be corrected by the Reed-Solomon forward error correction algorithm, which is part of the GBT protocol.

Front-end modules were irradiated at the CHARM facility at CERN. CHARM uses 24 GeV protons from the PS to create a mixed radiation environment. Two different levels of radiation rate were investigated: the lower(higher) one colliding the PS beam on Aluminum sieve(copper) target.

The error cross section did not change with overall integrated fluence (or integrated dose).



Summary and Outlook

The ngFEC FC7 firmware can simultaneously drive slow controls to 14 (12) I²C slaves and fast controls for each of the 6 SFP links to HF (HB/HE) front-end modules. Furthermore, ngFEC FC7 can remotely program front-end FPGAs through JTAG commands. The system has been tested in three test stands (CERN, DESY, and FNAL), in dedicated irradiation tests performed at the CHARM facility, and with real proton-proton collisions at CMS. Installation is foreseen during LHC EYETS 2016/17.

Links

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CMS HCAL Upgrade page

CMS HCAL ngFEC Twiki (CMS internal)

CMS HF and HE irradiation test at the CHARM facility at CERN

Topical Workshop on Electronics for Particle Physics - TWEPP
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