CMS HCAL Slow Control Upgrade

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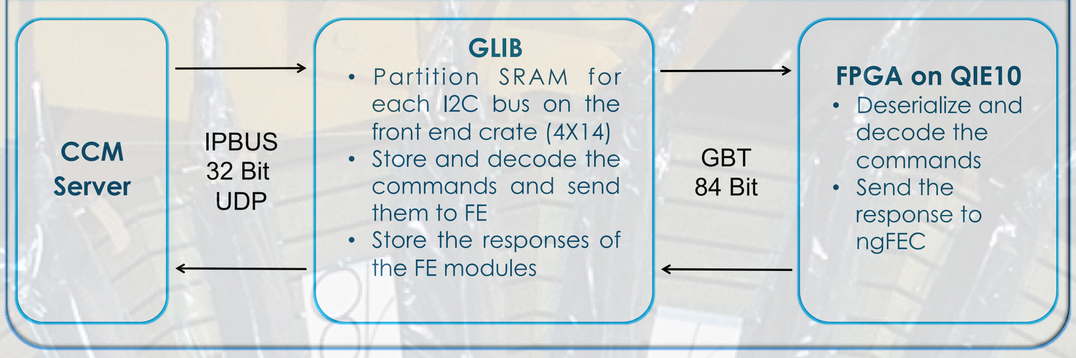
DESY

Introduction

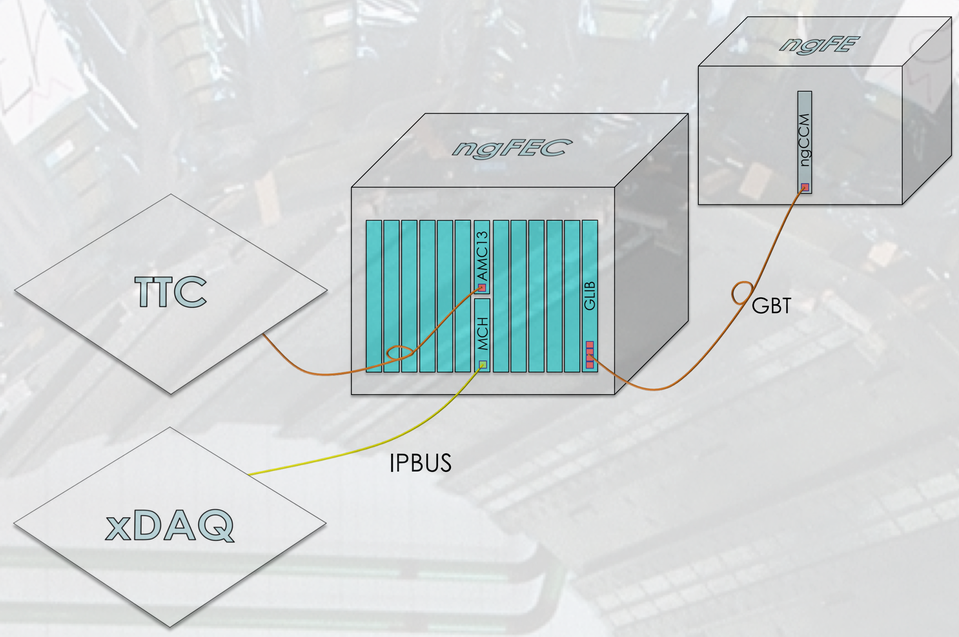
The CMS HCAL electronics will be upgraded to minimalize the potential of having maintainability and reliability problems due to **the lack of redundant connections** between different modules and the incapability of the old communication standard that has been used in the electronics infrastructure. With its 35 years old history **VME** has proven to be a suitable platform for high energy physics experiments; however, the standard is struggling to cope with the recent data transfer rates. Thus, it has been decided to change the current VME crates with **μTCA standard** which offers high speed data transfer rates through the backplane and redundant connections with **star topology**; in addition to these, with crate control hubs, it offers **better cooling solutions and power management** configurations. Specifications of the μTCA standard can be given as:

- The crate is controlled by a MCH, which can be accessible via USB or Ethernet connection.
- Through the MMCs on the modules MCH collects the temperature information of the modules and adjust the cooling level.
- In case of a failure, a μTCA crate stops delivering power (either for an AMC slot or over the crate) to prevent possible damages on the modules.
- All modules are **hot swappable** and and supported by a star topology.

Transaction Scheme



General Layout of the Slow Control System



Communication Protocols

There are 3 different communication protocols between CCM Server and ngCCM:

- **SiPM and QIE8 modules**: 2 I2C addresses per device (1 →Single I2C address and transfers 8 bytes of data) ADR for the pointer register and address ADR+1 as data register.
- **QIE10 FPGA**: Single I2C address and transfers 8 bytes of data.
- **GBTX**: Single I2C address but 2 byte of pointer must precede the data bytes.

The implementation in our system is as following:

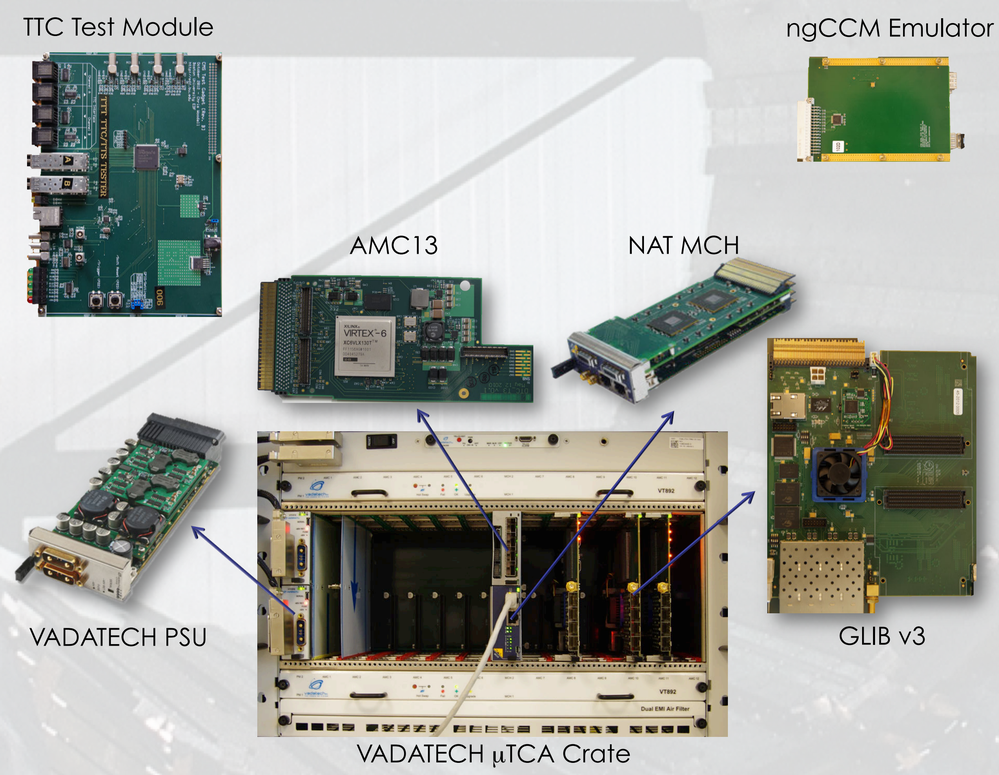
- **Command from the CCM Server**

Byte	Description
1	Transaction type → "0000RENN" R=1 → read R =0 → write E = 1 → if data register has I2C bus address is 1+ I2C address of pointer register E = 0 → if no extra I2C address for data NN → length of device internal register in bytes READ : • if TTCrx like → 1101 = 0xD, if QIE10 FPGA like → 1000 = 0x8, • if GBTX like → 1010 =0xA WRITE : • if TTCrx like → 0101 =0x5, • if QIE10 FPGA like → 0000 = 0x0, • if GBTX like → 0010 = 0x2
2	#bytes following
3	I2C bus number (actually known through buffer address)
4	#data bytes to write/read
5	Address on the I2C bus
6	Register number (length NN bytes (see byte 1 above))
…	Data bytes if write transaction (number given in byte 4)

- **Response from the ngFEC**

Byte	Description
1	ngCCM number
2	Status byte
3	#data bytes following (=0 for a write)
4	read data bytes

Setup at DESY



Conclusion & Future Plans

μTCA standard:

- Becoming a popular telecommunication standard in industry
- With its **advancements against the legacy systems**, is a suitable replacement for the current standard used in the CMS HCAL Electronics.

DESY CMS group is actively participating in this upgrade by developing the firmware and software for the μTCA ngFEC. A **test beam** is planned by the end of this year to check the compatibility of the complete Forward HCAL electronics upgrade layout. Therefore, finalizing the f/w and s/w for cDAQ→QIE10 communication is the prior goal to achieve. We would like to:

- Implement all 3 different ngCCM – CCM Server communication protocols to prevent compatibility problems.
- Test the distribution of **the TTC signal.**
- Build a **QIE10 emulator** which can respond to I2C interactions.

Modules

- **Advanced Mezzannine Card 13 (AMC 13):** Collects and distributes DAQ, TTC and TTS information to the modules within μTCA crate; developed by Boston University. The latest version is powered by a Kintex 7 and a Spartan 6 FPGA which also allows the AMC13 to achieve high speed (~10 Gbit/s) data transfers through the optical transceivers (SFPs).
- **Gigabit Link Interface Board (GLIB):** Evolution platform which provides gigabit SFP transceivers; developed by the CERN Electronics Department. The GLIB card is based on the Virtex 6 FPGA architecture.
- **MicroTCA Carrier Hub (MCH):** Crate control hub is responsible for the management of the crate and providing gigabit Ethernet link which enables access to modules in the crate through the backplane.
- **Power Supply:** Powers the entire crate: In our setup we have 2 redundant Vadatech PSU which feeds the ngFEC crate. Power delivery is managed by the MCH.
- **Charge Integrating Decoder 10 (QIE10)**: The new version of the previous Charge Integrating Decoder (QIE8) which has been used to sum and convert analog signals to digital signals in the CMS HCAL.
- **Next Generation Clock Control Module (ngCCM)**: The clocks will be distributed to the front end modules by ngCCM. It is a replacement for the old CCM module.
- **Module Management Controller (MMC)**: A small mezzanine card build around an Atmel Atmega 128 microcontroller and it can be placed on any kind of AMC module. It sends module information to the MCH and manage the connection between the AMC module and the μTCA crate.

Protocols

- **GBT**: Data transformation protocol which has been designed for use in the high energy particle physics experiments.
- **IPBUS**: Designed to establish a management connection between hardware and server computers. It mainly uses the UDP protocol.
- **I2C**: A two wire protocol which connects modules via relatively slow serial connection.

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CMS Compact Muon Solenoid

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